CLAIMS

What is claimed is:

1. An apparatus, comprising:

a signal selector circuit, which switches between providing an external clock signal or a feedback clock signal as an input clock signal to a delay line;

the delay line, coupled to the signal selector circuit, which receives the input clock signal and generates an internal clock signal; and

a feedback loop, coupled between an output of the delay line and an input of the signal selector circuit, which produces the feedback clock signal from the input clock signal.

2. The apparatus of claim 1, wherein the signal selector circuit comprises:

a phase detector, which receives the external clock signal and the feedback clock signal, and outputs a control signal based on a magnitude of a phase difference between the external clock signal and the feedback clock signal; and

a multiplexer, which provides the external clock signal or the feedback clock signal as the input clock signal, based on a value of the control signal.

3. The apparatus of claim 1, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal;

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to produce a control signal based on a magnitude of a phase difference between the external clock signal and the feedback clock signal; and

a multiplexer, which provides the feedback clock signal, the delayed external clock signal or the late clock signal as the input clock signal, based on a value of the control signal.

4. The apparatus of claim 1, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal;

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to produce a control signal based on a magnitude of a phase difference between the external clock signal and the feedback clock signal;

a set of delay elements for delaying the feedback clock signal, the delayed external clock signal, and the late clock signal, by an amount of delay that increases a likelihood that a multiplexer is properly set, resulting in a first multiplexer input signal, a second multiplexer input signal, and a third multiplexer input signal; and

the multiplexer, which provides, based on a value of the control signal, the first multiplexer input signal, the second multiplexer input signal or the third multiplexer input signal as the input clock signal.

5. The apparatus of claim 1, wherein the signal selector circuit comprises:

a phase detector, which receives the external clock signal and the feedback clock signal, and outputs a control signal based on a magnitude of a phase difference between the external clock signal and the feedback clock signal; and

a phase mixer, which transitions between providing the external clock signal or the feedback clock signal as the input clock signal, based on a value of the control signal.

6. The apparatus of claim 1, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal;

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to produce a control signal based on a magnitude of a phase difference between the external clock signal and the feedback clock signal; and

a phase mixer, which transitions between providing the feedback clock signal, the delayed external clock signal or the late clock signal as the input clock signal, based on a value of the control signal.

7. The apparatus of claim 1, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal;

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to produce a control signal based on a magnitude of a phase difference between the external clock signal and the feedback clock signal;

a set of delay elements for delaying the feedback clock signal, the delayed external clock signal, and the late clock signal, by an amount of delay that increases a likelihood that a phase mixer is properly set, resulting in a first mixer input signal, a second mixer input signal, and a third mixer input signal; and

a phase mixer, which transitions, based on a value of the control signal, between providing the first mixer input signal, the second mixer input signal or the third mixer input signal as the input clock signal, based on a value of the control signal.

8. The apparatus of claim 1, further comprising:

a phase detector circuit, which receives the input clock signal and the feedback clock signal, determines a phase difference between the input clock signal and the feedback clock signal, and generates a control signal having a value that depends on the phase difference; and

a shift register, coupled to the phase detector circuit, which receives the control signal, and provides a delay control signal to the delay line to control the delay line.

9. The apparatus of claim 1, wherein the feedback loop comprises:

a feedback delay circuit, which applies a delay to the internal clock signal and provides the feedback clock signal.

10. An apparatus, comprising:

a delay line which receives an input clock signal and generates an internal clock signal;

a feedback loop, coupled to an output of the delay line, which produces a feedback clock signal from the input clock signal;

a phase detector, coupled to the feedback loop, which determines a phase difference between the input clock signal and the feedback clock signal, and produces a control signal;

a shift register, coupled to the phase detector, which receives the control signal and controls the delay line correspondingly; and

a signal selector circuit, coupled to the delay line and the feedback loop, which switches between a delay locked loop mode and a phase locked loop mode, wherein in the delay locked loop mode, the signal selector circuit provides an external clock signal as the input clock signal to the delay line, and in the phase locked loop mode, the signal selector circuit provides the feedback clock signal as the input clock signal to the delay line.

11. The apparatus of claim 10, wherein the signal selector circuit comprises:

a phase detector, which receives the external clock signal and the feedback clock signal, and determines which of the external clock signal or the feedback clock signal the signal selector circuit produces as the input clock signal.

12. The apparatus of claim 10, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to determine which of the feedback clock signal, the delayed external clock signal or the late clock signal the signal selector circuit produces as the input clock signal.

13. The apparatus of claim 10, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal, and if an edge of the delayed external clock signal occurs after a corresponding edge of the feedback clock signal but before a corresponding edge of the late clock signal, the phase detector causes the signal selector circuit to output the delayed external clock signal as the input clock signal.

14. The apparatus of claim 10, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal, and if an edge of the delayed external clock signal occurs before a corresponding edge of the feedback clock signal, the phase detector causes the signal selector circuit to output the feedback clock signal as the input clock signal.

15. The apparatus of claim 14, wherein the signal selector circuit outputs the feedback clock signal only if the external clock signal and the internal clock signal are synchronized.

16. The apparatus of claim 10, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal, and if an edge of the delayed external clock signal occurs after corresponding edge of the late clock signal, the phase detector causes the signal selector circuit to output the late clock signal as the input clock signal.

17. The apparatus of claim 16, wherein the signal selector circuit outputs the late clock signal only if the external clock signal and the internal clock signal are synchronized.

18. An apparatus, comprising:

a signal selector means for providing an input clock signal to a delay means, wherein the signal selector means switches between providing an external clock signal or a feedback clock signal as the input clock signal;

the delay means, coupled to the signal selector means, for receiving the input clock signal and generating an internal clock signal; and

a feedback means, coupled between the delay means and the signal selector means, the feedback means for producing the feedback clock signal from the input clock signal.

19. The apparatus of claim 18, wherein the signal selector means switches between providing the external clock signal or the feedback clock signal based on a magnitude of a phase difference between the external clock signal and the feedback clock signal.

20. The apparatus of claim 18, wherein the signal selector means comprises:

a jitter detection means, for receiving the external clock signal and the feedback clock signal, and outputting a first control signal having a value that depends on whether a jitter in the external clock signal falls within an acceptable range of jitter values; and

a switching means, coupled to the jitter detection means, for switching between providing the external clock signal or the feedback clock signal in response to the first control signal.

21. The apparatus of claim 20, wherein the switching means is further responsive to a second control signal, which indicates whether or not the internal clock signal is synchronized with the external clock signal, and wherein the switching means does not switch to providing the feedback clock signal if the second control signal indicates that the internal clock signal is not synchronized with the external clock signal.

22. The apparatus of claim 18, further comprising:

a means for determining whether a timeout period has expired, wherein the signal selector means switches to providing the external clock signal as the input signal when the timeout period has expired.

23. The apparatus of claim 18, further comprising:

a phase detector means for receiving the input clock signal and the feedback clock signal, comparing a phase of the input clock signal with a phase of the feedback clock signal, and generating a control signal having a value that depends on a phase difference; and

a delay controller means for receiving the control signal, and providing a delay control signal to the delay means to control the delay means.

24. An apparatus, comprising:

a signal selector means for providing an input clock signal to a delay means, wherein the signal selector means selectively switches between providing an external clock signal or a feedback clock signal as the input clock signal, wherein the signal selector means provides the feedback clock signal as the input clock signal when a jitter in the external clock signal does not fall within an acceptable range of jitter values;

the delay means, coupled to the signal selector means, for receiving the input clock signal and generating an internal clock signal; and

a feedback means, coupled between the delay means and the signal selector means, the feedback means for receiving the input clock signal and generating the feedback clock signal.

25. The apparatus of claim 24, wherein the signal selector means delays and provides the feedback clock signal at a time that is later than an expected time of the external clock signal when the jitter causes the external clock signal to occur after the expected time by a value that exceeds a deviation threshold.

26. The apparatus of claim 24, wherein the signal selector means provides the feedback clock signal at a time that is earlier than an expected time of the external clock signal when the jitter causes the external clock signal to occur before the expected time by a value that exceeds a deviation threshold.

27. A clock synchronization circuit comprising:

a signal selector circuit, which switches between providing an external clock signal or a feedback clock signal as an input clock signal to a delay line;

the delay line, coupled to the signal selector circuit, which receives the input clock signal and generates an internal clock signal; and

a feedback loop, coupled between an output of the delay line and an input of the signal selector circuit, which produces the feedback clock signal from the input clock signal.

28. The clock synchronization circuit of claim 27, wherein the signal selector circuit comprises:

a phase detector, which receives the external clock signal and the feedback clock signal, and determines which of the external clock signal or the feedback clock signal the signal selector circuit produces as the input clock signal.

29. The clock synchronization circuit of claim 27, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to determine which of the feedback clock signal, the delayed external clock signal or the late clock signal the signal selector circuit produces as the input clock signal.

30. The clock synchronization circuit of claim 27, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal, and if an edge of the delayed external clock signal occurs after a corresponding edge of the feedback clock signal but before a corresponding edge of the late clock signal, the phase detector causes the signal selector circuit to output the delayed external clock signal as the input clock signal.

31. The clock synchronization circuit of claim 27, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal, and if an edge of the delayed external clock signal occurs before a corresponding edge of the feedback clock signal, the phase detector causes the signal selector circuit to output the feedback clock signal as the input clock signal.

32. The clock synchronization circuit of claim 27, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal, and if an edge of the delayed external clock signal occurs after corresponding edge of the late clock signal, the phase detector causes the signal selector circuit to output the late clock signal as the input clock signal.

33. The clock synchronization circuit of claim 27, further comprising:

a phase detector, coupled to the feedback loop, which determines a phase difference between the input clock signal and the feedback clock signal, and produces a control signal; and

a shift register, coupled to the phase detector, which receives the control signal and controls the delay line correspondingly.

34. An integrated circuit device, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit includes

a signal selector circuit, which switches between providing an external clock signal or a feedback clock signal as an input clock signal to a delay line,

the delay line, coupled to the signal selector circuit, which receives the input clock signal and generates an internal clock signal, and

a feedback loop, coupled between an output of the delay line and an input of the signal selector circuit, which produces the feedback clock signal from the input clock signal.

35. The integrated circuit device of claim 34, wherein the signal selector circuit comprises:

a phase detector, which receives the external clock signal and the feedback clock signal, and determines which of the external clock signal or the feedback clock signal the signal selector circuit produces as the input clock signal.

36. The integrated circuit device of claim 34, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to determine which of the feedback clock signal, the delayed external clock signal or the late clock signal the signal selector circuit produces as the input clock signal.

37. The integrated circuit device of claim 34, wherein the signal selector circuit further comprises:

a phase detector, coupled to the feedback loop, which determines a phase difference between the input clock signal and the feedback clock signal, and produces a control signal; and

a shift register, coupled to the phase detector, which receives the control signal and controls the delay line correspondingly.

38. An integrated circuit device, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein during operation, the integrated circuit performs a method that includes

receiving an external clock signal and providing the external clock signal to a delay line, which produces the internal clock signal,

providing a feedback clock signal from the internal clock signal,

comparing the external clock signal with the feedback clock signal to determine whether the external clock signal or the feedback signal is provided to the delay line based on whether a jitter in the external clock signal falls within an acceptable range of jitter values, and

if the jitter does not fall within the acceptable range, providing the feedback clock signal to the delay line rather than providing the external clock signal to the delay line.

39. The integrated circuit device of claim 38, wherein comparing the external clock signal with the feedback clock signal comprises:

delaying the external clock signal by a first delay to produce a delayed external clock signal;

delaying the feedback clock signal by a second delay to produce a late clock signal; and

comparing the feedback clock signal, the delayed external clock signal, and the late clock signal to determine whether an edge of the delayed external clock signal occurs

before a first corresponding edge of the feedback signal, between the first corresponding edge and a second corresponding edge of the late clock signal, or after the second corresponding edge.

40. The integrated circuit device of claim 38, wherein the feedback signal is provided to the delay line only if the external clock signal and the internal clock signal are synchronized.

41. An integrated memory circuit, comprising:

a substrate;

a plurality of memory cells supported by the substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit includes

a signal selector circuit, which switches between providing an external clock signal or a feedback clock signal as an input clock signal to a delay line,

the delay line, coupled to the signal selector circuit, which receives the input clock signal and generates an internal clock signal, and

a feedback loop, coupled between an output of the delay line and an input of the signal selector circuit, which produces the feedback clock signal from the input clock signal.

42. The integrated memory circuit of claim 41, wherein the signal selector circuit comprises:

a phase detector, which receives the external clock signal and the feedback clock signal, and determines which of the external clock signal or the feedback clock signal the signal selector circuit produces as the input clock signal.

43. The integrated memory circuit of claim 41, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to determine which of the feedback clock signal, the delayed external clock signal or the late clock signal the signal selector circuit produces as the input clock signal.

44. The integrated memory circuit of claim 41, wherein the signal selector circuit further comprises:

a phase detector, coupled to the feedback loop, which determines a phase difference between the input clock signal and the feedback clock signal, and produces a control signal; and

a shift register, coupled to the phase detector, which receives the control signal and controls the delay line correspondingly.

45. A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit includes

a signal selector circuit, which switches between providing an external clock signal or a feedback clock signal as an input clock signal to a delay line,

the delay line, coupled to the signal selector circuit, which receives the input clock signal and generates an internal clock signal, and

a feedback loop, coupled between an output of the delay line and an input of the signal selector circuit, which produces the feedback clock signal from the input clock signal.

46. The semiconductor die of claim 45, wherein the signal selector circuit comprises:

a phase detector, which receives the external clock signal and the feedback clock signal, and determines which of the external clock signal or the feedback clock signal the signal selector circuit produces as the input clock signal.

47. The semiconductor die of claim 45, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to determine which of the feedback clock signal, the delayed external clock signal or the late clock signal the signal selector circuit produces as the input clock signal.

48. The semiconductor die of claim 45, wherein the signal selector circuit further comprises:

a phase detector, coupled to the feedback loop, which determines a phase difference between the input clock signal and the feedback clock signal, and produces a control signal; and

a shift register, coupled to the phase detector, which receives the control signal and controls the delay line correspondingly.

49. An electronic system comprising:

a memory controller; and

an integrated memory circuit coupled to the memory controller, wherein the integrated memory circuit includes

a plurality of memory cells, and

an integrated circuit, wherein the integrated circuit includes

a signal selector circuit, which switches between providing an external clock signal or a feedback clock signal as an input clock signal to a delay line,

the delay line, coupled to the signal selector circuit, which receives the input clock signal and generates an internal clock signal, and

a feedback loop, coupled between an output of the delay line and an input of the signal selector circuit, which produces the feedback clock signal from the input clock signal.

50. The electronic system of claim 49, wherein the signal selector circuit comprises:

a phase detector, which receives the external clock signal and the feedback clock signal, and determines which of the external clock signal or the feedback clock signal the signal selector circuit produces as the input clock signal.

51. The electronic system of claim 49, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to determine which of the feedback clock signal, the delayed external clock signal or the late clock signal the signal selector circuit produces as the input clock signal.

52. The electronic system of claim 49, wherein the signal selector circuit further comprises:

a phase detector, coupled to the feedback loop, which determines a phase difference between the input clock signal and the feedback clock signal, and produces a control signal; and

a shift register, coupled to the phase detector, which receives the control signal and controls the delay line correspondingly.

53. An electronic system comprising:

a source of an external clock signal; and

an integrated memory circuit coupled to the source, wherein the integrated memory circuit includes

a signal selector circuit, which switches between providing an external clock signal or a feedback clock signal as an input clock signal to a delay line,

the delay line, coupled to the signal selector circuit, which receives the input clock signal and generates an internal clock signal, and

a feedback loop, coupled between an output of the delay line and an input of the signal selector circuit, which produces the feedback clock signal from the input clock signal.

54. The electronic system of claim 53, wherein the signal selector circuit comprises:

a phase detector, which receives the external clock signal and the feedback clock signal, and determines which of the external clock signal or the feedback clock signal the signal selector circuit produces as the input clock signal.

55. The electronic system of claim 53, wherein the signal selector circuit comprises:

a first delay element, which delays the external clock signal by a first delay to produce a delayed external clock signal;

a second delay element, which delays the feedback clock signal by a second delay to produce a late clock signal; and

a phase detector, which receives and compares the feedback clock signal, the delayed external clock signal, and the late clock signal to determine which of the feedback clock signal, the delayed external clock signal or the late clock signal the signal selector circuit produces as the input clock signal.

56. The electronic system of claim 53, wherein the signal selector circuit further comprises:

a phase detector, coupled to the feedback loop, which determines a phase difference between the input clock signal and the feedback clock signal, and produces a control signal; and

a shift register, coupled to the phase detector, which receives the control signal and controls the delay line correspondingly.

57. A method for generating an output clock signal, the method comprising:

receiving a first clock signal;

determining if a jitter in the first clock signal is within an acceptable range of jitter values;

if the jitter is within the acceptable range, delaying the first clock signal to produce the output clock signal; and

if the jitter is not within the acceptable range, delaying a second clock signal to produce the output clock signal.

58. The method of claim 57, wherein determining if the jitter is within the acceptable range comprises:

determining if an edge of the first clock signal occurs within a jitter window derived from the second clock signal;

if the edge occurs within the jitter window, determining that the jitter is within the acceptable range; and

if the edge occurs outside the jitter window, determining that the jitter is not within the acceptable range.

59. The method of claim 57, wherein the second clock signal is a feedback signal derived from the output clock signal, the method further comprising:

if the jitter is not within the acceptable range, determining whether the output clock signal is synchronized with the first clock signal before delaying the second clock signal to produce the output clock signal.

60. A method for generating an internal clock signal, the method comprising:

receiving an external clock signal and a feedback clock signal, wherein the feedback signal is derived from the internal clock signal;

determining whether a jitter in the first clock signal falls within an acceptable range of jitter values;

if the jitter falls within the acceptable range, delaying the external clock signal to produce the internal clock signal and the feedback clock signal; and

if the jitter does not fall within the acceptable range, delaying the feedback clock signal to produce the internal clock signal and the feedback clock signal.

61. The method of claim 60, wherein determining whether the jitter falls within the acceptable range comprises:

determining if an edge of the external clock signal occurs within a jitter window derived from the feedback clock signal;

if the edge occurs within the jitter window, determining that the jitter falls within the acceptable range; and

if the edge occurs outside the jitter window, determining that the jitter does not fall within the acceptable range.

62. The method of claim 60, further comprising:

if the jitter does not fall within the acceptable range, determining whether the internal clock signal is synchronized with the external clock signal before delaying the feedback clock signal to produce the internal clock signal.

63. A method for generating an internal clock signal, the method comprising:

receiving an external clock signal and providing the external clock signal to a delay line, which produces the internal clock signal;

providing a feedback clock signal from the internal clock signal;

comparing the external clock signal with the feedback clock signal to determine whether the external clock signal or the feedback signal is provided to the delay line based on whether a jitter in the external clock signal falls within an acceptable range of jitter values; and

if the jitter does not fall within the acceptable range, providing the feedback clock signal to the delay line rather than providing the external clock signal to the delay line.

64. The method of claim 63, wherein comparing the external clock signal with the feedback clock signal comprises:

delaying the external clock signal by a first delay to produce a delayed external clock signal;

delaying the feedback clock signal by a second delay to produce a late clock signal; and

comparing the feedback clock signal, the delayed external clock signal, and the late clock signal to determine whether an edge of the delayed external clock signal occurs before a first corresponding edge of the feedback signal, between the first corresponding edge and a second corresponding edge of the late clock signal, or after the second corresponding edge.

65. The method of claim 64, wherein providing the feedback clock signal comprises:

providing the feedback clock signal as the feedback clock signal if the edge of the delayed external clock signal occurs before the first corresponding edge of the feedback clock signal.

66. The method of claim 64, wherein providing the feedback clock signal comprises:

providing the late clock signal as the feedback clock signal if the edge of the delayed external clock signal occurs after the second corresponding edge of the late clock signal.

67. The method of claim 63, wherein the feedback signal is provided to the delay line only if the external clock signal and the internal clock signal are synchronized.

68. The method of claim 63, further comprising:

determining whether a switching condition has occurred; and

if the switching condition has occurred, providing the external clock signal to the delay line.

69. The method of claim 68, wherein the switching condition is the expiration of a timeout period.